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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/087,824	03/05/2002	Takumi Yamaguchi	60188-480	5180

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EXAMINER	
NGUYEN, LUONG TRUNG	
ART UNIT	**PAPER NUMBER**
2622	

DATE MAILED: 08/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/087,824	YAMAGUCHI ET AL.	
	Examiner	Art Unit	
	LUONG T. NGUYEN	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-4,14 and 15* is/are allowed.

6)☒ Claim(s) *5,8,10-13 and 16-19* is/are rejected.

7)☒ Claim(s) *6,7,9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claim 5 filed 6/13/2006 have been fully considered but they are not persuasive.

2. Applicant's arguments with respect to claim 16 and newly added claims 17-19 filed on 6/13/2006 have been considered but are moot in view of the new ground(s) of rejection.

In re page 10, Applicants argue that JP'070 fails to disclose or suggest corresponding low-level voltages at the gates of the alleged read 117a and reset 116a transistors being in the manner set forth in claim 5.

In response, regarding claim 5, Applicants recited the limitation "a low level voltage applied to a gate of said read transistor of each pixel is set to voltage lower than a low level voltage applied to a gate of said reset transistor thereof." Since the claim does not specifically define "a low level voltage", the Examiner read broadly this limitation as "a voltage." Note that the voltage applied to the gate of the read transistor 117a is OFF and the voltage applied to the gate of reset transistor 116a is ON when charge stored in detecting element is read out to the signal line 111. This means that a voltage applied to a gate of the read transistor 117a is set to voltage lower than a voltage applied to a gate of the reset transistor 116a, figure 10.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 5 is rejected under 35 U.S.C. 102(b) as being anticipated by Ihara et al. (JP 10-093070).

Regarding claim 5, Ihara discloses a solid state image sensor (solid state camera, see Abstract, figure 10, paragraph [0008]) comprising a plurality of amplifying unit pixels arranged two-dimensionally on a semiconductor substrate, each of said plurality of amplifying unit pixels including a photoelectric conversion region (photodiode 115a, figure 10, paragraph [0008]) for subjecting incident light to photoelectric conversion; a read transistor (address transistor 117a, figure 10, paragraph [0008]) for reading signal charge obtained through the photoelectric conversion; a storage region (detecting element, which corresponds to floating diffusion FD, figure 10, paragraph [0008]) for storing said signal charge read by said read transistor; a detect transistor (magnification transistor 114a, figure 10, paragraph [0008]) for detecting said signal charge on the basis of application of potential of said storage region to a gate thereof; a reset transistor (reset transistor 116a, figure 10, paragraph [0008]) for resetting said signal charge stored in said storage region; and a drain region (drain line 112, figure 10, paragraph [0008]) for supplying a pulse voltage to said storage region through said reset transistor,

wherein a read pulse for said read transistor of a first pixel out of said plurality of amplifying unit pixels and a reset pulse for said reset transistor of a second pixel adjacent to said

first pixel in a column direction are supplied through a common gate line (a read pulse for address transistor 117b and a reset pulse for reset transistor 116a are supplied through common gate line 113a, figure 10, paragraph [0008], and see Abstract), and

a LOW level voltage applied to a gate of said read transistor of each pixel is set to voltage lower than a LOW level voltage applied to a gate of said reset transistor thereof (since the claim does not specifically define "a low level voltage", the Examiner read broadly this limitation as "a voltage." Note that the voltage applied to the gate of the read transistor 117a is OFF and the voltage applied to the gate of reset transistor 116a is ON when charge stored in detecting element is read out to the signal line 111. This means that a voltage applied to a gate of the read transistor 117a is set to voltage lower than a voltage applied to a gate of the reset transistor 116a, figure 10).

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claim 16 is rejected under 35 U.S.C. 102(e) as being anticipated by Masuyama (US 7,057,655).

Regarding claim 16, Masuyama discloses a solid state image sensor (amplifying solid-state imaging device, figure 2) comprising a plurality of amplifying unit pixels arranged two-dimensionally on a semiconductor substrate, each of said plurality of amplifying unit pixels

including a photoelectric conversion region (photodiode 21, figures 2, 21) for subjecting incident light to photoelectric conversion; a read transistor (transistor TRi, figure 21, column 13, lines 32-44) for reading signal charge obtained through the photoelectric conversion; a storage region (storage node connected to capacitor 55, figure 21) for storing said signal charge read by said read transistor; a detect transistor (transistor 23, figures 2, 21) for detecting said signal charge on the basis of application of potential of said storage region to a gate thereof; a reset transistor (reset transistor RSi, figure 21) for resetting said signal charge stored in said storage region; and a drain region (VDD, figures 9, 21) for supplying a pulse voltage to said storage region through said reset transistor,

wherein said drain regions of said plurality of amplifying unit pixels are connected to a single drain layer also working as a light blocking film (the power line VDD 260 is made of a light blocking metal film, figure 9, column 10, lines 15-41),

wherein said single drain layer is formed above lines for connecting said storage regions to the gate of said detect transistors in said plurality of amplifying unit pixels and above signal lines for connecting to said detect transistors of said plurality of amplifying unit pixels (since power line VDD 260 blocks light incident on pixel 2 except photodiode 21, the power line VDD 260 is disposed on the top of pixel 2, that means the power line VDD 260 is above line connected storage node to gate of transistor 23 and signal line 6, figures 9, 21, column 10, lines 15-41).

Regarding claim 17, Masuyama discloses wherein said detect transistors of said plurality of amplifying unit pixels are connected to different lines column by column (figure 2).

Regarding claim 19, Masuyama discloses the single drain layer works as a cell shielding film of an optical black part (since power line VDD 260 blocks light incident on pixel 2 except photodiode 21, it works as a cell shielding film of an optical black part, column 10, lines 15-41).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 8, 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ihara et al. (JP 10-093070) in view of Gowda (US 6,115,066).

Regarding claims 8, 10, Ihara et al. discloses wherein said detect transistors of said plurality of amplifying unit pixels are connected to different signal lines column by column (magnification transistors 114a, 114b, 114c on each column are connected to each signal line 111, figure 10, paragraph [0008]).

Ihara et al. fails to specifically disclose said drain regions of said plurality of amplifying unit pixels are connected to different drain lines row by row, and said drain line and said signal line are disposed to cross each other in different layers.

However, Gowda et al. teaches a CMOS image sensor, in which the drain regions VR of plurality pixels 30 are connected to different drain lines 34i row by row (figures 3, 4) and drain line 34i column bus 15j (signal line) are disposed cross each other in different layers (figures 3,4). Therefore, it would have been obvious to one of ordinary skill in the art at the time the

invention was made to modify the device in Ihara et al. by the teaching of Gowda et al. in order to reduce the size of a pixel of an image sensor. This reduces the size of the image sensor.

Regarding claim 11, Ihara et al. discloses wherein a line for connecting said storage region to a gate of said detect transistor is made from a first light blocking metal layer (paragraph [0039]).

Regarding claim 12, Ihara et al. and Gowda et al. disclose wherein a line for connecting said storage region to a gate of said detect transistor and said drain line are made from a first metal layer above said gate line, and said signal line is made from a second metal layer above said first metal layer (note that Ihara discloses the signal lines and the drain lines are made of metal in paragraph [0039], and Gowda et al. discloses the drain lines 34i and signal line 35j are disposed cross each other in different layers in figures 3-4).

Regarding claim 13, Ihara et al. discloses wherein a line for connecting said storage region to a gate of said detect transistor and said signal line are made from a first metal layer above said gate line, and said drain line is made from a second metal layer above said first metal layer (figures 10-11).

9. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Masuyama (US 7,057,655) in view of Kochi (US 6,947,088).

Regarding claim 18, Masuyama fails to specifically disclose wherein said lines for connecting said storage regions to the gates of said detect transistors work as another light blocking film. However, Kochi teaches a solid-state image pickup element in which the FD line connects the storage node to the gate of transistor 2 is made of metal (column 2, lines 45-59, figures 1-2). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device in Masuyama by the teaching of Kochi in order to block incident light on the storage node. Doing so, the signal read out from storage node has less smear.

Allowable Subject Matter

10. Claims 1-4, 6-15 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claims 1-4, 6-15, see Examiner' statement of reasons for allowance as indicated in paper mailed on 3/13/2006.

11. Claims 6-7, 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to LUONG T. NGUYEN whose telephone number is (571) 272-7315. The examiner can normally be reached on 7:30AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID L. OMETZ can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LN
08/18/06

LUONG T. NGUYEN
PATENT EXAMINER